Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **I/P A1**
2. **I/P B1**
3. **O/P 1**
4. **I/P A2**
5. **I/P B2**
6. **O/P 2**
7. **GND**
8. **O/P 3**
9. **I/P B3**
10. **I/P A3**
11. **O/P 4**
12. **I/P B4**
13. **I/P A4**
14. **VCC**

**.050”**

**1 14 13**

**2**

**3**

**4**

**5**

**6 7 8**

**12**

**11**

**10**

**9**

**MASK**

**REF**

**M**

**0**

**0**

**8**

**X**

**.047”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004”**

**Backside Potential: GND**

**Mask Ref: M008X**

**APPROVED BY: DK DIE SIZE .047” X .050” DATE: 2/7/23**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54F08**

**DG 10.1.2**

#### Rev B, 7/1